Novel Transistor Type - The Magristor - and Novel Processor Type - Amperage Division Count and Latency Analysis Work Hand-in-Glove for Revolutionary Matrix Computing

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**Introduction**

In a conventional computer processor's architecture, individual pipelines are used to carry current to the myriad transistors of the architecture with extensive efforts made to prevent leaking of current out of these pipelines or out of the transistors themselves.

This traditional approach to processing is limited in many ways, one of which is that signals must exit the processor the way they enter and that each transistor is used, at most, a single time in each computational cycle.  The possibility of using a transistor multiple times in a cycle through the use of multiple, overlapping clocks governed by sub-processors within pins which are capable of modulating the frequency of injected signals was proposed upon 22 June 2023 (ibid.)

**Abstract**

In addition to performing concurrent computational steps at different clock speeds upon a shared architecture, discrete computational functions could additionally be executed upon the same architecture concurrently by using conductive two-dimensional planes as the connective medium between specialized, non-traditional transistors rather than insulated pipelines.  While individual two-dimensional planes would continue to be insulated from one another, transistors on the same plane would not be.

Electrons would be conveyed from three transverse directions (as from three of six sides of an hexagon) with an eye toward mere general control of angular momentum so that electrons would flow toward opposing sides of the processor where computational results could be collected.  In a traditional architecture, it would be to difficult to ensure computational usefulness without exacting control over electron flow via prescribed pipelines through which electrons are both conducted and restricted so as to ensure the arrival of electrons arrive at subsequent transistors.  In a two-dimensional transistor plane (integrated with the conductive plane) computation is a fault-tolerant process in which any transistor may assume responsibility for computational work without adversely affecting the integrity of the computational output.

This paradigm is made feasible through the advanced knowledge of the time of signal injection versus the time of signal output with femtosecond accuracy

(entirely feasible using the most novel atomic clocks, which are energy-efficient, compact and accurate to within a few attoseconds per year.)

While relative signal strength can be used to determine which output signal originated from which input, the distortion (femtosecond scale) to the arrival time of those electrons can be used to uniquely identify which transistors were in the "on" or "off" positions for electrons flowing in that particular direction.

Rather than relying upon the property of semiconduction, such a novel system would utilize semiconductors chosen for their magnetic properties. A high degree of ephemerality would be desired as in any semiconductor, but the presence/absence of electrical charge in such a transistor would not be essential to its mode of function. Each *magristor* would sit at a junction between sections of hexagonal boron-nitride would would naturally be Y-shaped with three paths being possible between any of the six-sided sections. It would only be natural for the overall processor to be hexagonal in shape. Further recursive function is made possible through atomically-thin pins directing input signals through stacked, discrete 2-D layers. Each computational cycle in this proposed system would therefore operate physically as a matrix does conceptually. This fact makes this processor design extremely efficient for the code-breaking functionality.

Each magristor would act as a multi-directional switchtrack mechanism and would be capable of handling electrons flowing from three different directions. Only the magnetic orientation of the side of a magristor facing toward the oncoming electrons would be able to affect the trajectory of electrons flowing from that direction.

A group of electrons striking a single prong of a three-pronged magristor that is magnetized on the relevant side would be bidirectionally redirected whilst a group of electrons striking the same prong when it is non-magnetized would be inducted by the mechanism, being therefore pushed only in a single direction and not undergoing a division of signal strength.

Tapered electrical dampening would be utilized to ensure that no two points on a pin/contact would inject current of the same amplitude into any two injection points, with amplitude diminishing along a predictable gradient along the length of the 2D pins. Amplitude at exit would be used to determine how many divisions of current have transpired with regard to each specific injection of current. The amperage of injection at each injection point would itself be a prime value in order to preclude the possibility of any two injected signals having the same overall output strength as another.

Through meta-analysis of both the number of divisions undergone by each electrical impulse (of which there would be hundreds of thousands per facet, per layer) and the arrival time, the precise series of magristors and their on/off states could be extrapolated, with that configuration representing the computational "output" as opposed to a more traditional processor whereby

outputs are directly represented.  In this scheme, outputs are inferred rather than being stated explicitly.

## Conclusion

The ability to utilize the same processing architectures to perform two functions concurrently is a step toward improving overall efficiency.  The aforementioned design would likely be application-specific, but revolutionary within the context of that application.